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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/885,553	06/20/2001	Lars-Peter Heineck	GR 98 P 1379 D	6319
24131	7590	02/25/2005	EXAMINER	
LERNER AND GREENBERG, PA			MONDT, JOHANNES P	
P O BOX 2480			ART UNIT	
HOLLYWOOD, FL 33022-2480			PAPER NUMBER	
			2826	

DATE MAILED: 02/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/885,553	Applicant(s) HEINECK ET AL.	
	Examiner Johannes P. Mondt	Art Unit 2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 1/21/05 (RCE) and 12/14/04 (1.116).
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,3,7 and 8 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,3,7 and 8 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on January 21, 2005 has been entered.

Response to Amendment

Amendment After Final Rejection filed December 14, 2004 has been entered following aforementioned Request for Continued Examination. In said Amendment Applicant cancelled claim 4, including the further limitation thereof in independent claim 1, thus substantially amending claims 3 and 8. Claims 1, 3, 7 and 8 are pending.

Comments on Remarks in said Amendment are included below under "Response to Arguments".

Response to Arguments

2. Applicant's arguments filed as Remarks in said Amendment After Final Rejection filed December 14, 2004 have been fully considered but they are not persuasive. In particular, the following comments are offered in response.

(a) With regard to the traverse based on the distinction between passivation and spacer (pages 5 and 6 of said Remarks):

A “passivation” layer is a thin oxide layer to protect against contamination or shorts. Thus the passivation layer on the gate side wall by Applicant does not distinguish from the “spacer” 136 in this regard, because spacer 136 is a thin oxide layer on the side walls of the gate which by virtue of its material constitution (oxide) and geometrical and topographical delineation protects the gate material from shorts (Please note that refractory metal silicide layer 114 abuts said “spacer” 136) and contamination by its blanket cover over regions 124, 126, 114 and 116 of varied material constitution. That said “spacer” indeed is also used as spacer for the ion implantation step described in column 5 is another matter and irrelevant to the determination whether or not said “spacer” is a passivation layer. Counter to the allegation in the final line of the first paragraph on page 6 of Remarks there is no material distinction between the “oxide passivation layer” and the layer 136 identified by the previous office action as passivation layer: both are disclosed as silicon oxide layers (see Ahmad, col. 5, l. 13-21 and claim 5 in col. 6, l. 48-49).

(b) With regard to the traverse based on the alleged non-conductive properties of the refractory metal silicide (pages 6-7):

Applicant misinterprets the adjective “isolating” in column 3, lines 34-35 in Ahmad to mean “electrically isolating”. Refractory metal silicides are inherently electrically conductive, with which Applicant evidently agrees (page 7, lines 12-14). “Isolating” within the context of Ahmad therefore cannot possibly mean electrically isolating.

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Instead it clearly refers to a function of the refractory metal silicide to isolate atoms or ions rather than electrons. Indeed, refractory metal silicides including tungsten silicide specifically are known for their isolating, i.e., barrier, function as witnessed, for instance, by Hung et al (5,965,035): see polysilicon layer 12 and silicon nitride cap layer 16 with tungsten silicide barrier layer 14 in between, within gate structure 12 (Figure 1 and col. 1, l. 63 – col. 2, l. 12). Only a handful of metals are refractory. The inclusion as tungsten as an equivalent refractory metal over any other refractory metal in a refractory metal silicide layer as barrier layer, i.e., isolating (isolating on the atomic level, not the electronic level, to avoid re-occurrence of the confusion by Applicant), layer between a polysilicon lower gate layer and a silicon nitride cap layer is thus well established in view of Hung et al, and hence case law such as in Re: Leshin 125 USPQ 416, as cited below is well justified.

For the above reasons the examiner must disagree with Applicant's conclusory allegation on page 8 of said Remarks (first paragraph).

Finally and parenthetically, counter to Applicant's allegation (page 9) that it "is noted that claim 1 does not raise new issues that would require further search because the added feature, which is from previous claim 4, has already been considered by the examiner", Applicant is reminded that the simultaneous claim limitations of the plurality of features now included in claim 8 disprove aforementioned Applicant's allegation, because said plurality of features has never before been presented to the examiner. Moreover, the omission of polysilicon as alternative material selection from the claim

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language as previously formulated in claim 4 substantially narrows the invention now claimed.

Claim Objections

3. ***Claim 3*** objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim, or amend the claim to place the claim in proper dependent form, or rewrite the claim in independent form. In particular, the further limitation "said gate includes a layer selected from the group consisting of a tungsten silicide layer and a polysilicon layer" (claim 3) does not further limit claim 1 which already contains the limitation "said gate including a tungsten silicide layer and a polysilicon layer".

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

1. **Claim 1** is rejected under 35 U.S.C. 103(a) as being unpatentable over Ahmad (6,037,639) in view of Hung et al (5,965,035).

Ahmad teaches (cf. Figure 5 and title, abstract, col. 1, l. 5-10, col. 3, l. 11 – col. 5, l. 50):

a semiconductor substrate 101 (col. 3, l. 19-23) having a substrate surface (upper main surface) (cf. Figure 5), a first conductive region and a second conductive region, namely: source and drain regions 117 (col. 3, l. 37-48);

a gate oxide 108/124 (col. 3, l. 31-37 and col. 4, l. 16-32) disposed on said substrate surface;

a gate 112/114 (col. 4, l. 16-21) disposed on said gate oxide over an area between said first conductive region and said second conductive region and having side walls adjacent respective ones of said conductive regions (cf. Figure 5), said gate including a refractive metal silicide layer 114 (col. 3, l. 31-36) and a polysilicon layer 112 (col. 3, l. 31-36);

a silicon oxide passivation layer 136 (col. 5, l. 13-21) disposed on said sidewalls of said gate; and

an insulating silicon nitride spacer 138 (col. 5, l. 44-50) disposed on said silicon oxide passivation layer, said spacer inherently acting as an oxidation barrier by virtue of its material constitution and location (the limitation “said spacer acting as...” constitutes functional language and does not further limit the MOS transistor as device);

said gate oxide insulating said gate from said semiconductor substrate (because said gate oxide is interposed between said gate and said substrate; cf. Figure 5) and having a thickened area 124 (col. 4, l. 16-32) in a region below at least one (in fact both) of said side walls adjacent said conductive regions (cf. Figure 5).

Ahmad does not necessarily teach the further limitation that the metal of said refractory metal silicide layer to be the refractory metal *tungsten*. *However, it would have been obvious to include said further limitation* because within the context of refractory metal silicides as barrier, i.e., isolating, layers tungsten silicide is well known in the art, as witnessed by Hung et al, who in a patent including gates structures 18 teach as prior art the selection of tungsten silicide as barrier layer 14 between polysilicon layer 12 and silicon nitride cap layer 16 (cf. col. 1, l. 63-col. 2, l. 12 and Figure 1). Applicant is reminded in this regard that it has been held that mere selection of known materials generally understood to be suitable to make a device, the selection of the particular material being on the basis of suitability for the intended use, would be entirely obvious. In re Leshin 125 USPQ 416.

On claim 3: the further limitation as defined by claim 3 is met (see discussion above of claim 1) and fails to further limit the claim, a fortiori thus is seen not to distinguish over the prior art: said gate already includes a layer selected from the group consisting of a tungsten silicide layer and a polysilicon layer because said gate includes a tungsten silicide layer and a polysilicon layer (loc.cit.).

2. **Claim 7** is rejected under 35 U.S.C. 103(a) as being unpatentable over Ahmad and Hung et al as applied to claim 4, and further in view of Krautschneider ((5,854,500). As detailed above, claim 4 is unpatentable over Ahmad in view of Hung et al. Ahmad nor Hung et al necessarily teach the further limitation of claim 7. However, it would have been obvious to include said further limitation in view of Krautschneider: as shown by Krautschneider (front figure), lateral MOS transistors with attributes as taught by Ahmad, particularly with gate oxide 110 (see in Krautschneider column 5, lines 17-26 and column 6, lines 26-27) and nitride side spacers 114 (cf. column 6, lines 45-49), and with a gate of polysilicon (cf. column 5, lines 19-20), for instance, have long been applied as selection transistors to DRAM memory cells (cf. abstract, first sentence), thus constituting an obvious use of the invention by Ahmad. It has to be kept in mind that *motivation* to combine the references also derives from the stated field of application to random access memory devices made by Ahmad (see Ahmad, col. 1, l. 5-10).

3. **Claim 8** is rejected under 35 U.S.C. 103(a) as being unpatentable over Ahmad (6,037,639 B1) and Hung et al as applied to claim 1 above, and further in view of Krautschneider ((5,854,500). As detailed above, claim 1 is unpatentable over Ahmad et al in view of Hung et al. Ahmad does not necessarily teach the further limitation of claim 8. However, it would have been obvious to include said further limitation in view of Krautschneider: as shown by Krautschneider (front figure), lateral MOS transistors with attributes as taught by Ahmad, particularly with gate oxide 110 (see in Krautschneider

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column 5, lines 17-26 and column 6, lines 26-27) and nitride side spacers 114 (cf. column 6, lines 45-49), and with a gate of polysilicon (cf. column 5, lines 19-20), for instance, have long been applied as selection transistors to DRAM memory cells (cf. abstract, first sentence), thus constituting an obvious use of the invention by Ahmad. It has to be kept in mind that *motivation* to combine the references also derives from the stated field of application to random access memory devices made by Ahmad (see Ahmad, col. 1, l. 5-10).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P. Mondt whose telephone number is 571-272-1919. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J. Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).


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JPM

February 17, 2005

Patent Examiner: 

Johannes Mondt (Art Unit: 2826).